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MAYER, BROWN, ROWE & MAW LLP
1909 K STREET, N.W.
WASHINGTON, DC 20006

EXAMINER	
LIN, PHYOWAI	
ART UNIT	PAPER NUMBER
2112	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,988	KIM ET AL.	
	Examiner	Art Unit	
	PHYOWAI LIN	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/19/04,09/02/05,10/10/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The references listed in the Information Disclosure Statement filed on March 19,2004 and September 02,2005 and October 10, 2006 have been considered by the examiner (see attached PTO-1449 form or PTO/SB/08A and 08B forms).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claim 1,3,4,6-11,13-18 and 20** are rejected under 35 U.S.C. 102(b) as being anticipated by Ido et al. (US Pub Number 2002/0181853).

Regarding to claim 1, Ido et al. discloses an optical transceiver (see [0114] lines 2 and FIG.19), comprising:

a photoelectric transducer (LD module-see [0019] line 1 and FIG. 2) implemented on a substrate (a silicon sub-mount 8-see [0050] line2 and FIG. 2) and having a light transmitting device (a laser diode(LD) element 9-see [0048] line 2 and FIG.2) for converting an electrical signal into a light signal (see [0048] line 2-3) ,

a high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device, a bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device, a light receiving device (PD element 10-see [0079] line 3 and FIG.9) for converting the light signal into the electrical signal (see [0079] lines 1-3) , a high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device, a bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device, a first dummy ground line (ground pin 6-3-see [0049] line16 and FIG.2) located adjacent to the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device, and a second dummy ground line (lead 6-4-see [0079] line 8 and FIG.9) located adjacent to the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device; and

a light signal transmitter (a LD driver IC 112-see [0114] line 7 and FIG.19) connected to the photoelectric transducer (a LD module-see [0114] line 2 and FIG.19), transmitting a light signal received from an optical fiber to the light receiving device (see [0114] lines 13-17 in which light transmits from LD module which enters into the fiber first and then is received by PD module), and transmitting a light signal generated from the light transmitting device to the optical fiber (see [0014] line 9-13) .

Regarding to claim 3, Ido et al. discloses everything claimed as applied above (see claim 1). In addition, the optical transceiver includes:

wherein the first dummy ground line (ground pin 6-3-see [0049] line16 and FIG.2) is located between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device (see FIG.2 in which the ground pin 6-3 is placed between a microstrip line 3-9 and the electrode pattern 3-11); and

the second dummy ground line (lead 6-4-see [0079] line 8 and FIG.9) is located between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device (see FIG.9 in which lead 6-4 is placed between around the perimeter of a strip line 3-9 and the electrode pattern 3-12).

Regarding to claim 4, Ido et al. discloses everything claimed as applied above (see claim 1). In addition, the optical transceiver includes:

wherein the light transmitting device (a LD module-see [0048] line 1 and FIG.1) is a laser diode (a laser diode (LD) element 9-see [0048] line2 and FIG.1) and the light receiving device (PD module-see [0079] line 2 and FIG.9) is a photo diode (PD element 10-see [0079] line 3 and FIG.9).

Regarding to claim 6, Ido et al. discloses everything claimed as applied above (see claim 1). In addition, the optical transceiver includes:

wherein the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device is located between the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device and the first dummy ground line (ground pin 6-1-see [0049] line16 and FIG.2) and also (see FIG2 in which a microstrip line 3-9 is placed between the ground pin 6-1 and the electrode pattern 3-11) ; and

the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device is located between the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device and the second dummy ground line (lead 6-2-see [0079] line 8 and FIG.9) and also (see FIG.9 in which a strip line 3-9 is placed between around the perimeter of lead 6-2 and the electrode pattern 3-12).

Regarding to claim 7, Ido et al. discloses everything claimed as applied above (see claim 6). In addition, the optical transceiver includes:

wherein the space between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the first dummy ground line (ground pin 6-1-see [0049] line16 and FIG.2) is less than or equal to the space between

the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device (see FIG.2 in which the distance between a microstrip line 3-9 and ground pin 6-1 is smaller than the distance between a microstrip line 3-9 and electrode pattern 3-11); and

the space between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the second dummy ground line (lead 6-2-see [0079] line 8 and FIG.9) is less than or equal to the space between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device (see FIG.9 in which the distance between a strip line 3-9 and lead 6-2 is smaller than the distance between the perimeter of a strip line 3-9 and the electrode pattern 3-12).

Regarding to claim 8, Ido et al. discloses everything claimed as applied above (see claim 6). In addition, the optical transceiver includes:

wherein the first (ground pin 6-1-see [0049] line16 and FIG.2) and the second dummy ground lines (lead 6-2-see [0079] line 8 and FIG.9) are located outside the photoelectric transducer (see FIG 2 and FIG 9 in which both ground lines are placed outside the LD module and PD module); and

the bias lines (electrode pattern 3-11-see [0070] line 4 and FIG.2 and the electrode pattern 3-12-see [0079] line 14 and FIG.9)) for the light transmitting device and the light receiving device are located inside the photoelectric transducer (see FIG.2 and FIG.9 in which both bias lines are placed inside the LD module and PD module).

Regarding to claim 9, Ido et al. discloses everything claimed as applied above (see claim 1). In addition, the optical transceiver includes:

wherein the photoelectric transducer (LD module-see [0019] line 1 and FIG. 2) further comprises a monitor photo detector (MPD) (a monitor PD element 10-see [0068] line 2) and a monitor photo detector (MPD) signal line for monitoring optical power of the light transmitting device (see [0068] line 2-3).

Regarding to claim 10, Ido et al. discloses everything claimed as applied above (see claim 9). In addition, the optical transceiver includes:

wherein the first dummy ground line (ground pin 6-3-see [0049] line16 and FIG.2) is located between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device (see FIG.2 in which the ground pin 6-3 is placed between a microstrip line 3-9 and the electrode pattern 3-11); and

the second dummy ground line (lead 6-4-see [0079] line 8 and FIG.9) is located between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device (see FIG.9 in which lead 6-4 is placed between around the perimeter of a strip line 3-9 and the electrode pattern 3-12).

Regarding to claim 11, Ido et al. discloses everything claimed as applied above (see claim 9). In addition, the optical transceiver includes:

wherein the light transmitting device (a LD module-see [0048] line 1 and FIG.1) is a laser diode (a laser diode (LD) element 9-see [0048] line2 and FIG.1) and the light receiving device (PD module-see [0079] line 2 and FIG.9) is a photo diode (PD element 10-see [0079] line 3 and FIG.9).

Regarding to claim 13, Ido et al. discloses everything claimed as applied above (see claim 9). In addition, the optical transceiver includes:

wherein the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device is located between the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device and the first dummy ground line (ground pin 6-1-see [0049] line16 and FIG.2) and also (see FIG2 in which a microstrip line 3-9 is placed between the ground pin 6-1 and the electrode pattern 3-11) ; and

the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device is located between the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device and the second dummy ground line (lead 6-2-see [0079] line 8 and FIG.9) and also (see FIG.9 in which a strip line 3-9 is placed between around the perimeter of lead 6-2 and the electrode pattern 3-12).

Regarding to claim 14, Ido et al. discloses everything claimed as applied above (see claim 13). In addition, the optical transceiver includes:

wherein the space between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the first dummy ground line (ground pin 6-1-see [0049] line16 and FIG.2) is less than or equal to the space between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device (see FIG.2 in which the distance between a microstrip line 3-9 and ground pin 6-1 is smaller than the distance between a microstrip line 3-9 and electrode pattern 3-11); and

the space between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the second dummy ground line (lead 6-2-see [0079] line 8 and FIG.9) is less than or equal to the space between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device (see FIG.9 in which the distance between a strip line 3-9 and lead 6-2 is smaller than the distance between the perimeter of a strip line 3-9 and the electrode pattern 3-12).

Regarding to claim 15, Ido et al. discloses everything claimed as applied above (see claim 13). In addition, the optical transceiver includes:

wherein the first (ground pin 6-1-see [0049] line16 and FIG.2) and the second dummy ground lines (lead 6-2-see [0079] line 8 and FIG.9) are located outside the photoelectric transducer (see FIG 2 and FIG 9 in which both ground lines are placed outside the LD module and PD module); and

the bias lines (electrode pattern 3-11-see [0070] line 4 and FIG.2 and the electrode pattern 3-12-see [0079] line 14 and FIG.9)) for the light transmitting device and the light receiving device are located inside the photoelectric transducer (see FIG.2 and FIG.9 in which both bias lines are placed inside the LD module and PD module).

Regarding to claim 16, Ido et al. discloses everything claimed as applied above (see claim 1). In addition, the optical transceiver includes:

a package encapsulant (the metal cap5-see [0051] line6 and FIG.1) attached to the substrate (see [003] line 32 and FIG.1 where in the metal cap is joined to the substrate);

a leadframe pad (the electrode pattern 3-0-see[0051] line 7 and FIG.1) located inside the package encapsulant(see FIG.1 where in the electrode pattern is placed inside the metal cap); and

a plurality of leadframes (lead pins 6-1 through 6-8-see FIG.2 and FIG.9) connected to the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device, the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device, the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device, the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device, the first dummy ground line, the second dummy ground line, and the leadframe pad (the electrode pattern 3-0-see[0051] line 7 and FIG.1) and also (see FIG.2 and FIG.9 where in the lead pins are connected to mictrostrip line 3-9, electrode pattern 3-11, a strip line 3-9 and the electrode pattern 3-12) , respectively.

Regarding to claim 17, Ido et al. discloses everything claimed as applied above (see claim 16). In addition, the optical transceiver includes:

wherein the first dummy ground line (ground pin 6-3-see [0049] line16 and FIG.2) is located between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device (see FIG.2 in which the ground pin 6-3 is placed between a microstrip line 3-9 and the electrode pattern 3-11); and

the second dummy ground line (lead 6-4-see [0079] line 8 and FIG.9) is located between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device (see FIG.9 in which lead 6-4 is placed between around the perimeter of a strip line 3-9 and the electrode pattern 3-12).

Regarding to claim 18, Ido et al. discloses everything claimed as applied above (see claim 16). In addition, the optical transceiver includes:

wherein the light transmitting device (a LD module-see [0048] line 1 and FIG.1) is a laser diode (a laser diode (LD) element 9-see [0048] line2 and FIG.1) and the light receiving device (PD module-see [0079] line 2 and FIG.9) is a photo diode (PD element 10-see [0079] line 3 and FIG.9).

Regarding to claim 20, Ido et al. discloses everything claimed as applied above (see claim 16). In addition, the optical transceiver includes:

wherein the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device is located between the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device and the first dummy ground line (ground pin 6-1-see [0049] line16 and FIG.2) and also (see FIG2 in which a microstrip line 3-9 is placed between the ground pin 6-1 and the electrode pattern 3-11) ; and

the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device is located between the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device and the second dummy ground line (lead 6-2-see [0079] line 8 and FIG.9) and also (see FIG.9 in which a strip line 3-9 is placed between around the perimeter of lead 6-2 and the electrode pattern 3-12).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ido et al. (US Pub Number 2002/0181853) in view of Ido et al. (US Pub Number 2003/0194192).

Regarding to claim 2, Ido et al. discloses everything claimed as applied above (see claim 1). However he fails to disclose what is the silicon substrate made of for better operating in optical communication.

Ido et al. (US Pub Number 2003/0194192). teaches the optical transceiver includes wherein the substrate (see [0027] line 15) is composed of a silicon substrate (see [0027] line 16) having a silicon oxide film (see [0027] line 16).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ido et al.'s invention as making the silicon substrate with the silicon oxide film on top of silicon substrate instead of using other chemical materials because insulation film of silicon oxide would not allow the current flow in the electrode of the photodiode and silicon oxide film itself has its own capacitance.

7. **Claim 5,12 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ido et al. (US Pub Number 2002/0181853) in view of Terada et al. (US Pub Number 2002/0027230)

Regarding to claim 5, Ido et al. discloses everything claimed as applied above (see claim 1). However he fails to disclose the optical transceiver has a planner lightwave circuit for all optical components are mounted on a common substrate to get efficiency coupling power to each other.

Terada et al. discloses where in the light signal transmitter (LED 12-see [0057] line 4) is composed of a planar lightwave circuit (PLC) (see [0029] lines1-3).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ido et al.'s invention as mounting the planar lightwave circuit on the substrate instead of using separate optical module circuits on substrate because the PLC platform hybrid integration circuit sets up all optical components on a common substrate and it makes optical coupling among them firm and stable against temperature variation. On the other hand, the integration of LD and PD to a common substrate increases optical and electrical coupling between them.

Regarding to claim 12, Ido et al. discloses everything claimed as applied above (see claim 9). However he fails to disclose the optical transceiver has a planner lightwave circuit for all optical components are mounted on a common substrate to get efficiency coupling power to each other.

Terada et al. discloses where in the light signal transmitter (LED 12-see [0057] line 4) is composed of a planar lightwave circuit (PLC) (see [0029] lines1-3).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ido et al.'s invention as mounting the planar lightwave circuit on the substrate instead of using separate optical module circuits on substrate because the PLC platform hybrid integration circuit sets up all optical components on a common substrate and it makes optical coupling among them firm and stable against temperature variation. On the other hand, the integration of LD and PD to a common substrate increases optical and electrical coupling between them.

Regarding to claim 19, Ido et al. discloses everything claimed as applied above (see claim 16). However he fails to disclose the optical transceiver has a planner lightwave circuit for all optical components are mounted on a common substrate to get efficiency coupling power to each other.

Terada et al. discloses where in the light signal transmitter (LED 12-see [0057] line 4) is composed of a planar lightwave circuit (PLC) (see [0029] lines1-3).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ido et al.'s invention as mounting the planar lightwave circuit on the substrate instead of using separate optical module circuits on substrate because the PLC platform hybrid integration circuit sets up all optical components on a common substrate and it makes optical coupling among them firm and stable against temperature variation. On the other hand, the integration of LD and PD to a common substrate increases optical and electrical coupling between them.

Citation of Pertinent Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kuhara et al. (US Patent Number 6614964) discloses an apparatus for including a transmitter and receiver modules help reducing electrical cross talk and noise during operation.

Nakanishi et al. (US Patent Number 6318908) discloses light transmitting and receiving module having a silicon substrate, fiber waveguide and filtering circuit for better optical communication.

Nakanishi et al. (US Patent Number 6374021) discloses LD /PD module which includes two fiber waveguides, laser diode, photo diode and monitoring photo diode for advanced optical communication.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHYOWAI LIN whose telephone number is (571) 270-1659. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo R. Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LIN

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1/7/07

ELISEO RAMOS-FELICIANO
SUPERVISORY PATENT EXAMINER